CLAIMS

What is claimed is:

1. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project a height above said active surface;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry;

applying an encapsulant material at least over said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements;

removing a depth of said encapsulant material sufficient to expose a portion of each of said intermediate conductive elements; and

placing said semiconductor substrate with said intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and

electrically connecting said intermediate conductive elements and said conductive bumps.

2. The method of claim 1, further including forming bond pads over the exposed portions of said intermediate conductive elements before electrically connecting said intermediate conductive elements to said conductive bumps.

3. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project a height above said active surface;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry;

applying an encapsulant material at least over said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements;

removing a depth of said encapsulant material sufficient to expose a portion of each of said intermediate conductive elements; and

forming conductive traces over said encapsulant material from said exposed portions of said intermediate conductive elements to at least one channel of said pattern of channels, defining a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced edge contacts therealong, and severing said semiconductor substrate in alignment with at least some of said channels including said at least one channel into a plurality of semiconductor elements each comprised of said at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material and said plurality of laterally spaced edge contacts are located along a peripheral edge of a semiconductor element of the plurality.

4. The method of claim 3, further comprising aligning said plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.

5. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project to a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced edge contacts therealong;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing said at least one individual die location and exposing said laterally spaced edge contacts of said peripheral edge;

applying an encapsulant material at least over said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements; and

severing said semiconductor substrate in alignment with at least some of said channels including said at least one channel into a plurality of semiconductor elements each comprised of said at least one individual die location, wherein said plurality of laterally spaced edge contacts are exposed along the peripheral edge of said individual die location.

6. The method of claim 5, further comprising aligning said plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.